Practise Set- I
Power Electronics (ELE 603)
Department of Electrical Engineering
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The following questions are meant for practice purpose. No submission is expected.

1) Draw a four quadrant switch (definition: resulting device has both positive & negative voltage blocking, along with positive & negative current conduction capabilities) using a few diodes & one IGBT.

2) A fully controlled switch is turned OFF in a circuit by withdrawing the gate pulse. The turn-off transition time of the device is $8\mu s$. During ON conditions, the device was carrying a current i = 10A, & the ON- state voltage drop was $V_{ON} = 0.2V$. Once it turned OFF the leakage current was observed to be $I_{leak} = 0.01A$, & the device was blocking a voltage of V = 230V . Determine the turn-OFF power loss ($P_{loss,off}$) if the device was oper- ated at a switching frequency of $f_{sw} = 2kHz$.

3) A thyristor is connected in a series RL circuit fed by a DC source of $100V$, with $R = 5\Omega$ & $L = 20mH$. If the latching current of the device is $10mA$, & the gate current is issued for a duration of $1\mu s$, determine whether the device will trigger or not.

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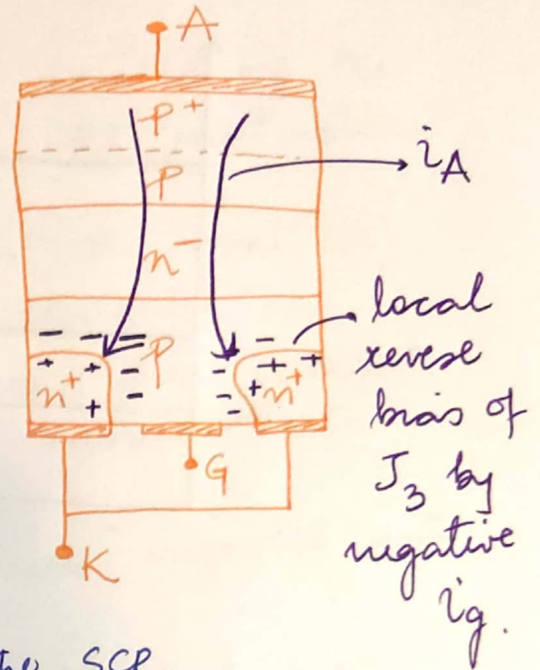
Why does negative gate current fail to turn off an SCR?



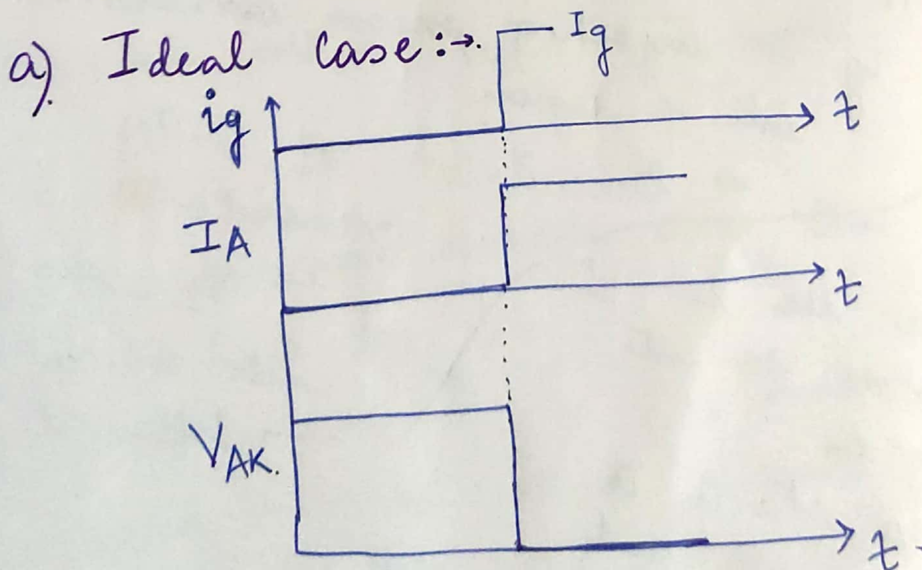
The high magnitude anode current flowing through the SCR continues to forward bias the junction J_3, while the minimal -ive i_g tries to reverse bias is locally and hence fails in turning off the SCR.

DYNAMIC CHARACTERISTICS OF SCR

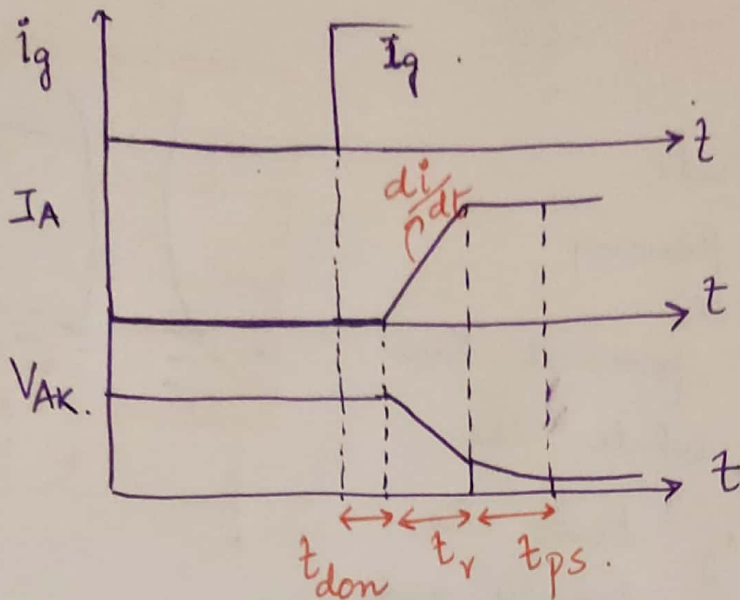
⇒ Response w.r.t time (Switching Characteristics)

1) TURN ON CHARACTERISTICS:

a) Ideal Case:→



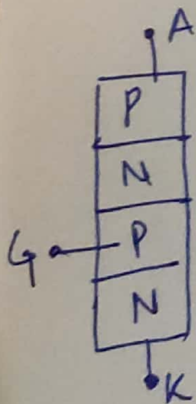
b) Practical case:→



Total $t_{on} = t_{don} + t_r + t_{ps}$.

- t_{don} ↓ turn ON delay time
- t_r ↓ rise time
- t_{ps} ↓ plasma spread time.

t_{doN} :→ thyristor appears to be off ⇒ V_{AK} ↑, i_A ↓



But i_g is injecting excess carriers into p region
⇒ Base drive of NPN transistor.
↳ Q_2 goes into saturation
↳ followed by Q_1.

Once the 2 transistors go into saturation
i_A starts to rise and
V_{AK} starts to fall.

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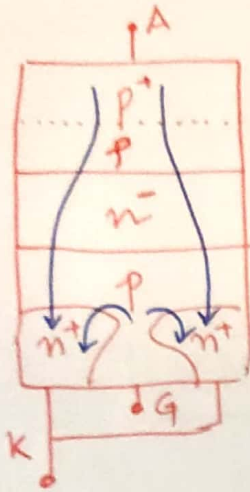
t_r : (Rise time)

Once the 2 transistors enter saturation anode current starts building up.
↳ rising at a rate $\frac{di}{dt}$ ⇒ decided by the ckt parameters.



Due to gate injection, the pn (GK) junction initially participates in the conduction process. This current starts spreading as current starts rising
⇒ more & more carriers injected into cathode.

2 phenomena happen simultaneously.
↳ current rises
↳ current spreads

Generally, the current rises faster than it spreads, and when the current reaches its ON-state value ⇒ rise time ends.

t_{ps} : (Spreading time).

As conduction spreads over the surface of SCR ⇒ V_{AK} ↓↓
After the end of t_r, i_A has risen to maximum value but hasn't spread.
∴ V_{AK} has'nt reduced to minimal value

The time taken for plasma spreading is t_{ps}.
(generally $t_{ps} > t_r$).

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$\frac{dI}{dt}$ and Protection

* If $\frac{di}{dt}$ is too high,

i_A attains max value very soon $\Rightarrow t_r << t_{ps}$.

which means a lot of current is being carried out through a small area $\Rightarrow$ hotspots.

$\Rightarrow$ heat $\Rightarrow$ thermal runaway

$\Rightarrow$ device burns.

For Protection:

i) ~~At manufacturing tech:~~

a) Increase the turn on area

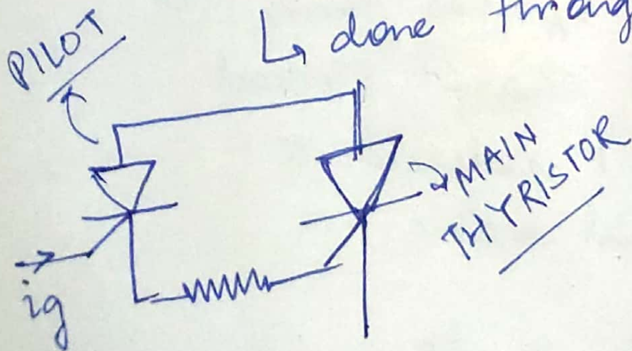
↓

* By using large i_g during t_{don} & t_r intervals

$\Rightarrow$ turn on area ↑

So generally i_g↑ in the beginning and it is gradually reduced.

↳ done through pilot thyristor.



→ Method 1 of increasing turn ON area.

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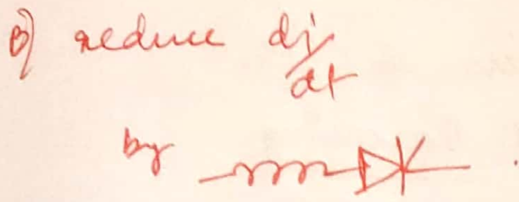
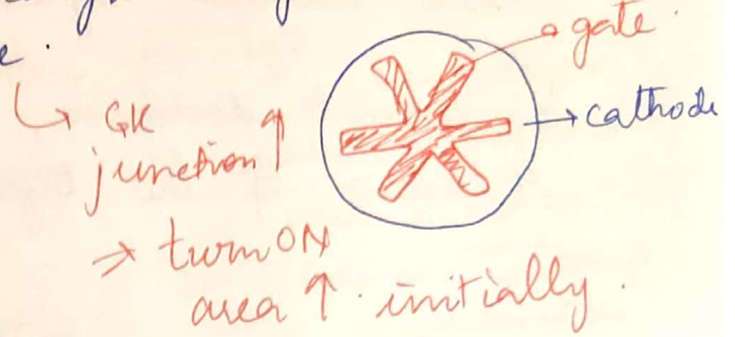
Method · II → Gate - cathode geometry is altered so as to increase the junction area · through interleaving or interdigitated gate cathode structure ·





2) TURN - OFF CHARACTERISTICS :

Gate has no role to play in the turn-off process ·

SCR is turned off using reverse-bias ·

$i_A(t)$, di/dt, t_{rr}, t, 0, $I_{rr}/4$, I_{rr}, dv_F/dt

$V_{AK}(t)$, t, 0, $t=0$, t_1, t_2, t_3, V_{Rev}, t_4

t_{doff}, t_{qr}, t_{rr}

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When applied voltage is decreased,
i_A starts decreasing at a ~~voltage~~ rate decided by ckt parameters.

As current decreases, excess carriers in the 4 layers of the thyristor start decreasing

- Internal recombination
- carrier sweep out

Current keeps decreasing to reach zero & keeps going in the negative direction, while voltage across the device remains still small ~~& still~~ positive, till J_1 or J_3 get reverse biased.

↓

This happens when the excess carrier density peak of the respective junction falls to zero.

Usually J_3 becomes reverse biased first typically when I_{rr} peaks in the negative direction. (reverse recovery current.)

By this time, carrier concentration is too less to sustain the negative current so it begins to ~~fa~~ reduce (-ve current) and ~~reduces~~ decays to zero.

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Also, once J_3 gets reverse biased, the ckt negative voltage kicks because of circuit inductance.

The inductive kick is determined by how fast -ive I_{rr} falls to zero.

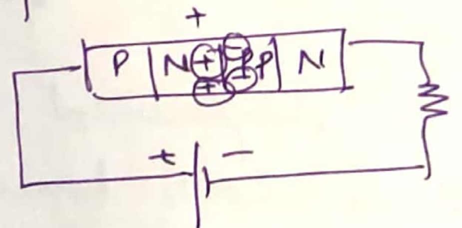
The -ive bias has to stay for t_{qr}

↳ charge recovery. ⇒ ~~minority~~ inner layer carriers are removed through internal re-combination.

Then F.B may be applied

$\frac{dV}{dt}$ and protection

When forward biased again at a rate dV/dt, a space charge potential (depletion layer) is set up at J_2

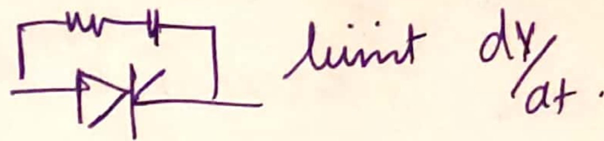


↳ Hence developing capacitance at J_2

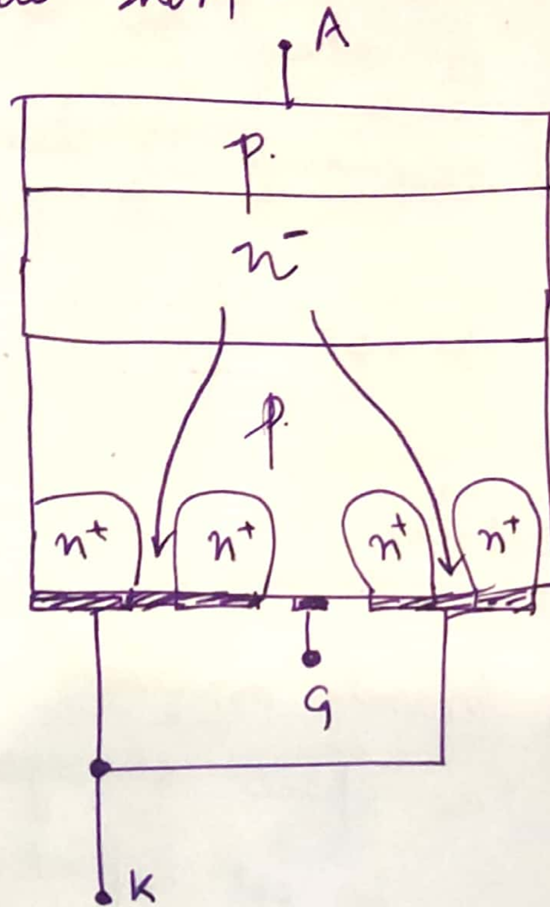
If $\left(C_{j2}\frac{dV}{dt}\right)$ is high, a displacement current I_{j2} max exceed break over current & spurious turn ON may occur. To prevent this,

$$\left.\frac{dV}{dt}\right|_{max} < \frac{I_{BO}}{C_{j2}}.$$

1) RC snubber ckt



2). Cathode short.



↳ displacement current intercepted by cathode. shorts hence preventing carrier injection into junction J_3 (n^+ region).

3) Use of interdigitated G-K structure.