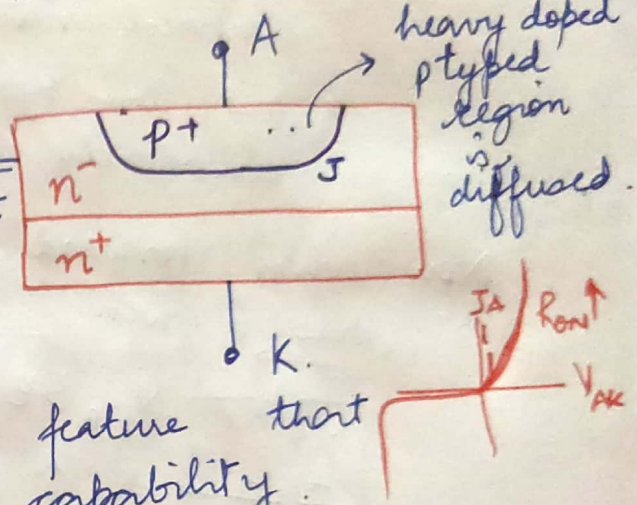
The Physics Behind Devices / operation Principles [LECTURE 3]

1) POWER DIODE

Modifications are made structurally to simple low-power diodes so as to make their high power equivalents.



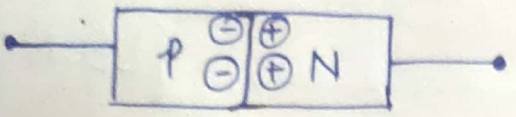
n^- layer is the primary feature that imparts high power capability.
↳ drift region.

* When reverse biased :-
(blocking high voltages)
⇒ carriers move away from junction
As doping concentration ↓.
⇒ thickness / penetration level of space charge / depletion region ↑.

* When Forward biased.
→ lightly doped n- region contributes heavily to increase in ohmic resistance. ⇒ loss ⇒ heat
⇒ hence heat sinks

* high current carrying capacity is possible due to large wafer dias.

Back ground:

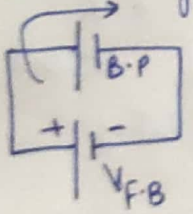


↳ due to migration of carriers, a mild barrier potential is set-up.

→ individually p and n loose their electrical neutrality.

→ But the system as a whole remains electrically neutral.

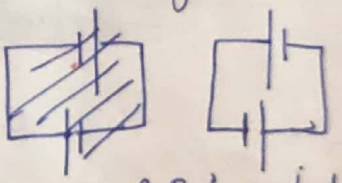
Now when Forward Bias is given



$V_{F.B} > B.P.$

$\Rightarrow i \uparrow$.

And when Reverse Bias is given



B.P is aided

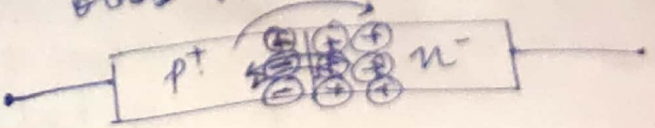
⇒ Depletion layer thickens.

By using an n^- epitaxial layer

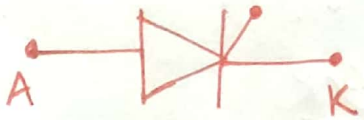
→ we increase the penetration depth of depletion layer.

How? 1 side (p^+) is heavy doped (high no of carriers/volume)

other side (n^-) is lightly doped (low no of carriers/volume)



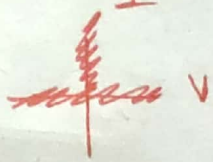
2) SILICON CONTROLLED RECTIFIER (Thyristor / SCR).



→ Bell ~~laboratories~~ (1950's) / GE research

→ 10kV, 6AkA ratings

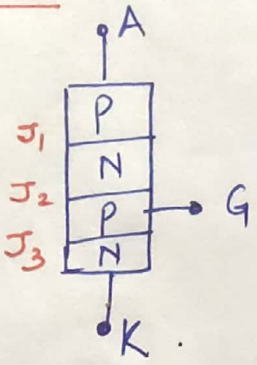
→ HVDC systems

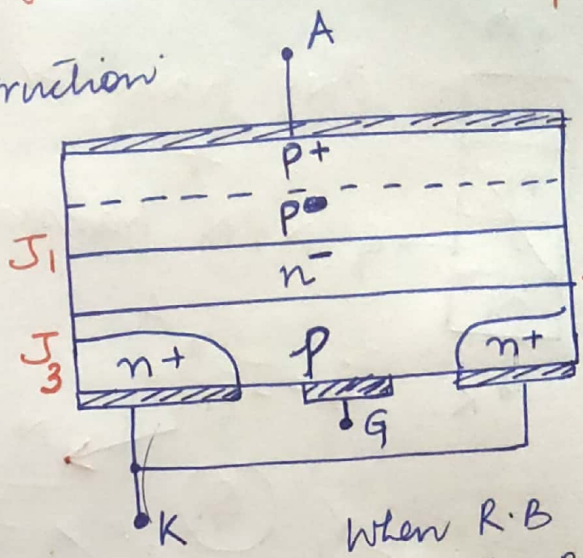


unidirectional

semi-controlled.

Structure:→ 4-layer construction





* When forward biased:→

$J_1 \Rightarrow$ F.B.

$J_2 \Rightarrow$ R.B ⇒ depletion layer ↑

↳ Blocking of forward voltage.

$J_3 \Rightarrow$ F.B.

When R.B Breakdown ← $J_1 \Rightarrow$ R.B, $J_3 \Rightarrow$ R.B, $J_2 \Rightarrow$ F.B

$V_{F.B}$ ↑ ⇒ Break Over is achieved ⇒ J_2 potential is overcome

not preferred { ⇒ Device goes into conduction

(Remember Break Over ≠ Break down).

preferred { $V_{F.B} < V_{BO}$.

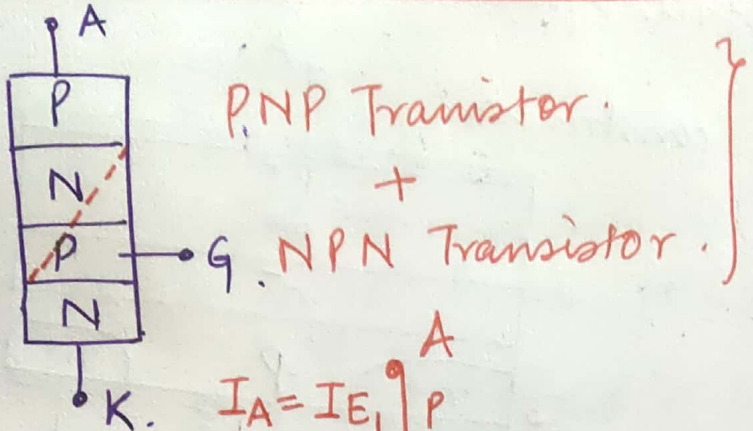
⇒ i_g is varied into the gate terminal.

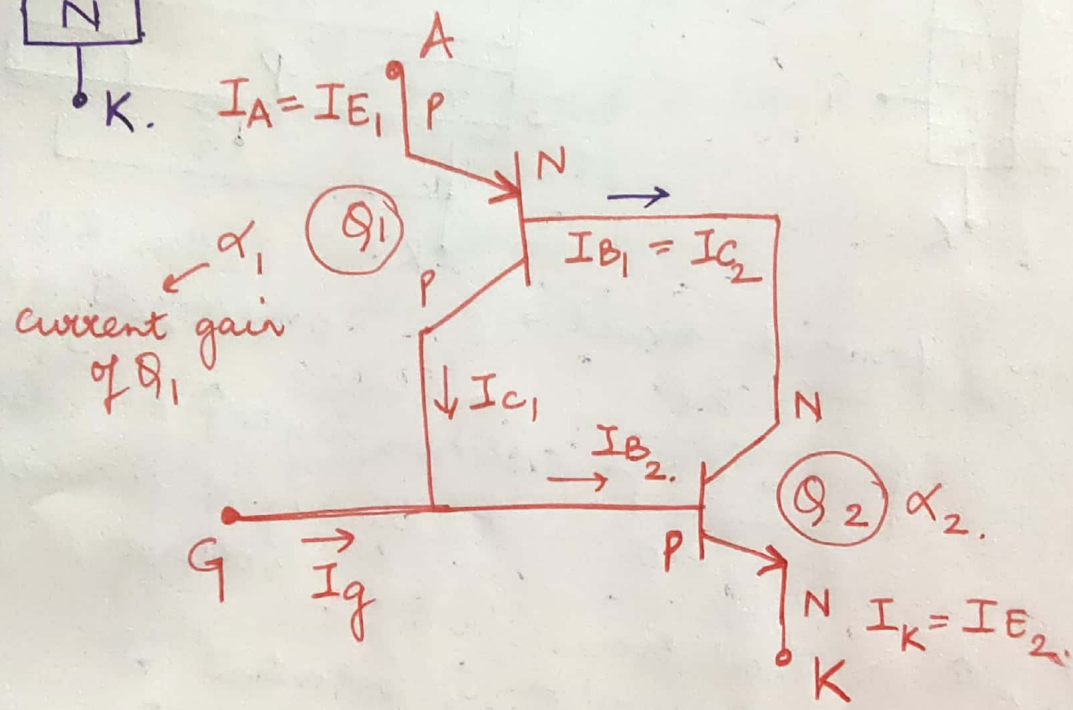
↳ goes into conduction.

Device physics →

how ig turns the device ON ?

TWO TRANSISTOR MODEL OF AN SCR.





Using Ebers Molls' equations,

$$I_{C_1} = \alpha_1 I_{E_1} + I_{CO_1} \quad \rightarrow (1)$$

$$I_{C_2} = \alpha_2 I_{E_2} + I_{CO_2} \quad \rightarrow (2)$$

$$\Rightarrow I_{C_1} = \alpha_1 I_A + I_{CO_1}$$

$$I_{C_2} = \alpha_2 I_K + I_{CO_2}$$

Assuming No Gate Signal to be present

$\Rightarrow$ $I_g = 0 \Rightarrow I_A = I_K$.

$I_{E_1} = I_{E_2} = I_A$ Adding ① and ②

$$I_{C_1} + I_{C_2} = (\alpha_1 + \alpha_2) I_A + I_{CO_1} + I_{CO_2}$$

$$\boxed{I_A = \frac{I_{CO_1} + I_{CO_2}}{1 - (\alpha_1 + \alpha_2)}}$$

α_1, α_2 very small in blocking state.

$\Rightarrow I_A$ has a minimal contribution owing to leakage currents $I_{CO_1} + I_{CO_2}$.

$V_{F\cdot B} \uparrow \Rightarrow I_{CO_1} \uparrow, I_{CO_2} \uparrow$.

At $V_{F\cdot B} = V_{BO}$.

$\rightarrow I_{C_1} \uparrow \Rightarrow$ Base drive for Q_2
$\Rightarrow$ goes into saturation
$\Rightarrow I_{C_2} \uparrow \Rightarrow$ Base drive for Q_1.
$\Rightarrow$ goes into saturation
$\Rightarrow I_{C_1} \uparrow$

$Q_1 \rightarrow Q_2 \rightarrow$ saturation

$\longrightarrow$ SCR has latched into conduction / triggered / fired.

Assuming $i_g \neq 0$.

$$i_A + i_g = i_K.$$

$$I_{C_1} + I_{C_2} = \alpha_1 I_A + \alpha_2 I_K + I_{CO_1} + I_{CO_2}.$$

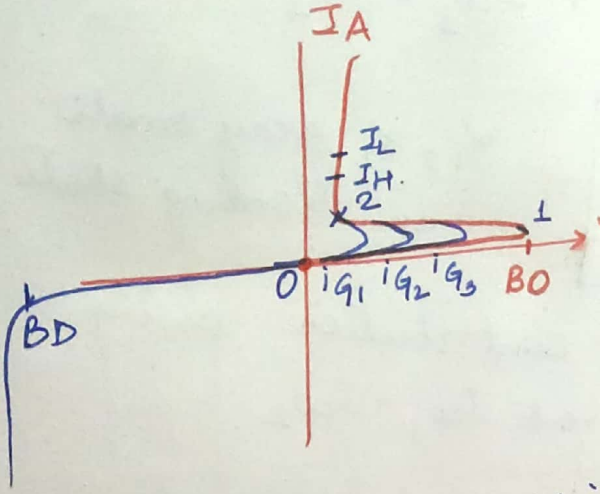
$$I_A - \alpha_1 I_A - \alpha_2 i_A - \alpha_2 i_g = I_{CO_1} + I_{CO_2}.$$

$$\boxed{I_A = \alpha_2 i_g + \frac{I_{CO_1} + I_{CO_2}}{1 - (\alpha_1 + \alpha_2)}}$$

$\Rightarrow$ initial base drive

V_{BO} not reached

STATIC VI characteristics of an SCR. LECTURE 4



$i_{G_1} > i_{G_2} > i_{G_3}$.

When F.B is applied.
⇒ no conduction.
0 to 1 ⇒ Forward Blocking region.
$V_{AK} \uparrow\uparrow$ and $I_A \approx 0$.

Until Break Over is reached
Once B.O is reached, SCR transitions from blocking to conduction state where $I \uparrow\uparrow$ and $V_{AK} \downarrow\downarrow\downarrow$.
↳ negative resistance region (1 to 2)
→ transitions too fast.

Finally conduction region.
⇒ Applied voltage ↑ ⇒ $I_A \uparrow$ ⇒ Vdrop almost constant.

Entire process is preponed ∵ gate

While turning ON

The minimum value of anode current reached, such that an SCR, withdrawal of gate pulse does not turn ~~the~~ device OFF again is called the latching current ⇒ Marks turn ON success.

While turning OFF an SCR, the $i_A \downarrow\downarrow$, the minimum value of i_A reached such that the device if F.B again will not go back into ~~reverse~~ conduction, is called holding current
→ Marks turn ~~OFF~~ success

⇒